Evaluation of Multilevel Memory Capability of ReRAM Using Ta_2O_5 Insulator and Different Electrode Materials

Yuanlin Li[1], Reon Katsumura[1], Mika Kristian Grönroos[1], Atsushi Tsurumaki-Fukuchi[1],
Masashi Arita[1], Hideyuki Andoh[2], Takashi Morie[2], and Yasuo Takahashi[1]
[1] Graduate School of Information Science and Technology, Hokkaido University, Sapporo 060-0814, Japan
[2] Graduate School of Life Science and Systems Engineering, Kyushu Institute of Technology, Kitakyushu 808-0196, Japan
Email: liyuanlin_nano@eis.hokudai.ac.jp

***Abstract* — ReRAM (Resistive Random Access Memory) has been drawing attention for its neural network applications with low-power and high-speed operation. The multilevel data storage capability is inherently needed to use the ReRAM as synaptic devices. In this study, two ReRAM devices with different electrode materials in which the operation mechanisms are thought to be different was fabricated and tested. It was clarified that the multilevel resistance characteristics were achieved in both devices.**

I. INTRODUCTION

The multilevel data storage capability of ReRAM has attracted much attention to realize simple neural network computing [1-3]. Multi-level resistance is thought to be realized by very thin metallic connection formed in an insulator layer of the ReRAM [4]. In general, there are two typical mechanisms for resistive switching; conductive bridge RAM (CBRAM) and valence change memory (VCM) [5]. CBRAM uses an active metal such as Cu that ionizes into the insulator and forms a Cu filament by means of redox reaction. On the other hand, VCM needs oxygen vacancies that flow into the insulator and form filaments. Although both mechanisms may provide multi-level operation capability, the ability of the two has not been discussed in detail.

In this study, multilevel memory characteristics of Ta oxide ReRAM devices with different top electrodes (TEs) of Cu and Ta were compared. Gradual and multilevel resistances were achieved by changing negative stop voltage during the reset process.

II. EXPERIMENT PROCESS

ReRAM devices are fabricated in a via hole as shown in Fig. 1. Metal layers were deposited by radio frequency sputtering. TaO_x thickness and gas condition (Ar/O_2 ratio) of superstring was properly controlled to achieve gradual reset process in the current−voltage (I−V) characteristics shown in Fig. 2. The TaO_x for Cu-TE is 7-nm thick and the Ar/O_2 ratio during sputtering was 100/0, and TaO_x for Ta-TE is 10-nm thick and Ar/O_2 ratio was 50/50.

III. RESULTS AND DISCUSSION

Forming or set process was performed by I−V scanning toward positive direction. Then the reset process was performed by changing negative stop voltage. Fig. 3 shows sequential I−V scanning characteristics for the Cu-TE device measured by increasing stop voltage toward negative direction. Multilevel resistances were successfully achieved in the halfway of the reset process. The results for the Ta-TE device are shown in Fig. 4, which shows basically similar characteristics to Cu-TE ones, though the mechanism of the filament formation is thought to be different. The resistances after voltage scan toward negative direction were plotted as a function of stop voltage in Fig. 5 for both Cu-TE and Ta-TE devices. It is interesting that the resistances are almost on the same line for both devices. Further clarification of the mechanism of conductive filament formation such as direct observation using *in-situ* TEM [6, 7] will provide useful information about this behavior.

Pulse operation for altering the ReRAM resistance is more suitable for neural network applications. A series of negative pulses with different pulse height and width were applied. Figs. 6 and 7 show resistance change after applying a series of negative voltage pulse with 100 μs wide and different heights for Cu-TE device and Ta-TE one, respectively. Fig. 7 summarizes the resistance of Ta-TE device as a function of pulse voltage height. The results clearly show that the higher negative pulses provide the higher resistances for both devices. In addition, gradual resistance increases were achieved after sequential pulse application, which may be able to moderate the resistance appropriately. It should be noted that the wider pulse width provided the faster resistance change and saturation, and shorter width caused slower changes.

IV. SUMMARY

It was proved that the multiple level resistance can be achieved by controlling the negative stop voltage applied during the reset process for both the Cu-TE and the Ta-TE/TaO_x ReRAMs, whereas the filament formation mechanisms are thought to be different. To obtain the desired resistance value, there are some options; such as pulse height, pulse width, and number of sequential pulses. It should be exanimated in upcoming research to clarify the underlying operation mechanisms.

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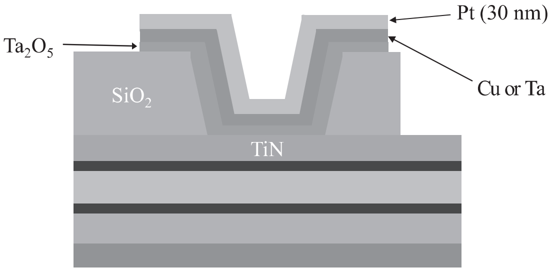

Fig .1. Schematic cross section of the device structure. After forming a via hole in SiO_2 layer, dielectric TaO_X was deposited on the TiN bottom electrode (BE) followed by the Cu or Ta top electrode (TE) and the Pt cover electrode.

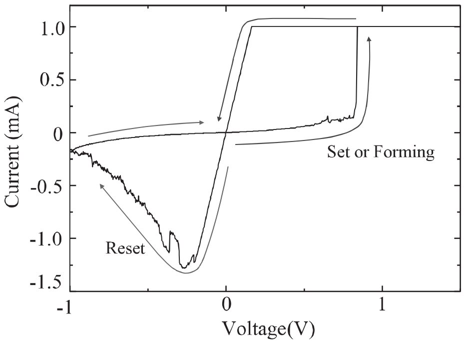

Fig. 2. *I*–*V* characteristics with a gradual reset that is promising for multilevel resistance.

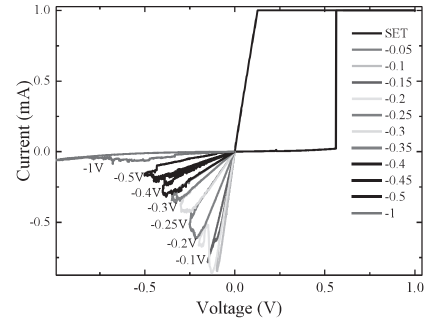

Fig. 3. A series of *I*–*V* scanning characteristics of a Cu-TE device during the reset process after set measured by increasing negative stop voltages. The stop voltages were changed from -0.05 V to -0.5V with steps of 0.05 V. To reset the devices completely, -1V was applied.

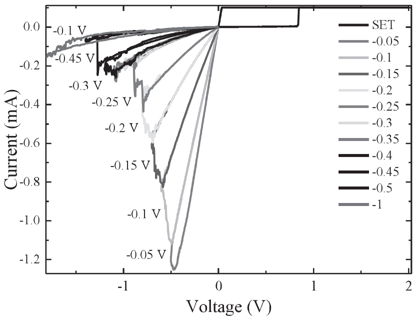

Fig. 4. A series of *I*–*V* scanning characteristics of a Ta-TE device during the reset process after set measured by increasing negative stop voltages. The stop voltages were changed from -0.5 V to -1.4 V with steps of 0.1 V. To reset the devices completely, -1.8 V was applied.

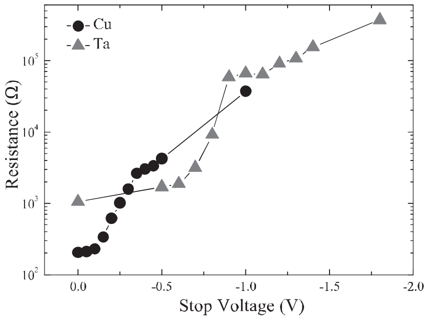

Fig. 5. Resistance of the Cu-TE and the Ta-TE devices as a function of stop voltage after negative *I*–*V* scans.

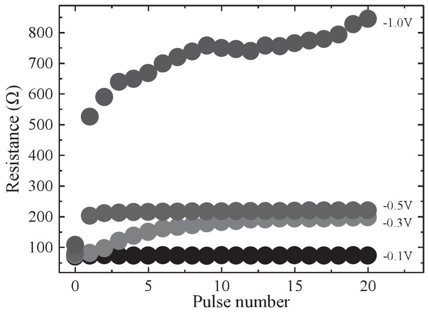

Fig. 6. Resistance of a Cu-TE device after applying a series of voltage pulses with different voltage heights. Pulse width was 100 µs.

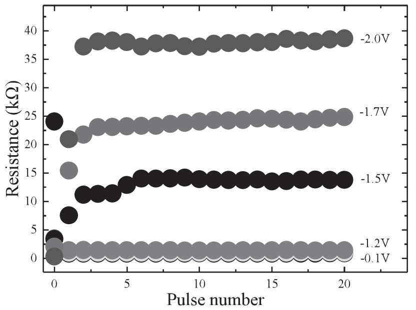

Fig. 7. Resistance of a Ta-TE device after applying a series of voltage pulses with different voltage heights. Pulse width was 100 µs.

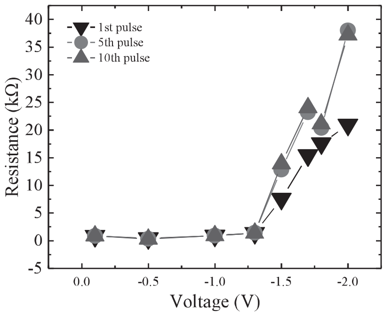

Fig. 8. Resistance of a Ta-TE device after applying a series of voltage pulses as a function of voltage heights. Pulse width was 100 µs.