Investigation on the RRAM Overshoot Current Suppression with Circuit Simulation

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Abstract — **In this paper, we have simulated how the overshoot current in the Resistive-switching Random Access Memory (RRAM) cell is generated and whether the integrated transistor can effectively suppress the overshoot current that can cause degradation of cell endurance. We propose a CMOS-friendly 1T1R fabrication process and proceed with circuit simulation using the process parameters. The simulation shows that the internal transistor effectively prevent RRAM overshoot current and be capable of controlling the compliance current.**

I. Introduction

RRAM (Resistive-switching Random Access Memory) has been widely studied as a device to overcome the limitations of existing nonvolatile memory. Advantages of RRAM include fast switching speed, high scalability, and simple structure [1], [2]. On the other hand, low reliability due to randomness and endurance problems need to be overcome, and so far, many studies have been done [3]-[5].

In this study, we point the overshoot current problem that could cause degradation in RRAM endurance [6]. We have designed an RRAM fabrication process and modeled the simulation circuit based on the parameters used in the designed process. We investigate the effect of internal transistor on overshoot current by comparing 1T1R and single RRAM (Fig. 1).

II. Simulation Results and Discussion

Transient simulation using 5 V square pulse was performed. When the voltage ramping proceeds 80 % of a rising time, SET transition from 1 MΩ to 1 kΩ occurs exponentially during 50 ns.

When SET transition occurs in single RRAM cell, voltage across the RRAM cell drops suddenly and discharging occurs in the cell capacitor and the external parasitic capacitor (Fig. 2a). The current due to this discharging flows instantaneously into the RRAM cell and causes current overshoot. Since the internal currents are offset from each other, the overshoot current above the compliance current cannot be detected by measuring equipment (Fig. 2b).

When SET transition occurs in 1T1R structure, voltage across the RRAM cell drops suddenly. However, in this case, supply voltage of the transistor connected in series with the RRAM is rapidly increased, which completely compensates the sudden voltage drop. Consequently the node voltage of external parasitic capacitor maintains (Fig. 3a).

Inside the RRAM, the transistor current and the discharging current of the internal capacitor flow. Externally measured current is the sum of the displacement current due to the external parasitic capacitor and the transistor current. RRAM cell is independent to the displacement current and only transistor current is actually acting on the RRAM cell (Fig. 3b, Fig. 3c).

By adjusting the gate voltage, transistor can act as a very finely controlled internal compliance current source in 1T1R structure (Fig. 4).

III. Summary

We have simulated circuit models of a 1T1R structure and a single RRAM structure. The simulation shows that 1T1R structure is effective enough to overcome the overshoot problem of the conventional single RRAM structure with external compliance current source.

Acknowledgement

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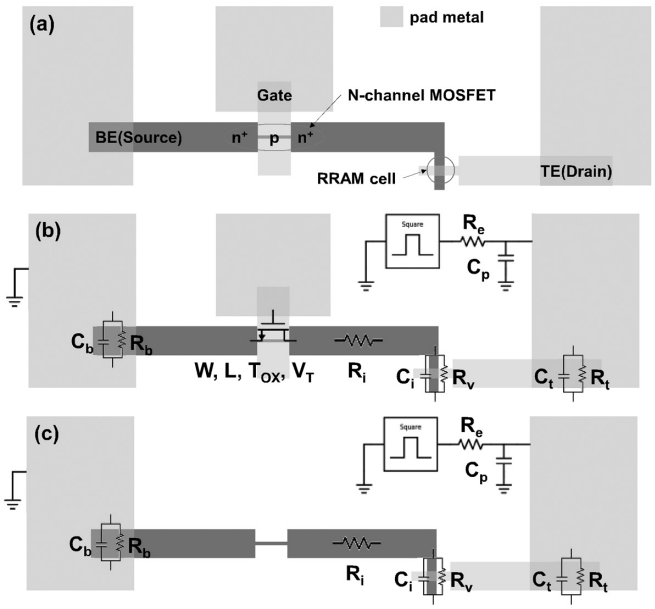

Fig. 1. Schematic top view of (a) proposed RRAM structure and (b) modeled circuit, (c) single RRAM circuit structure.

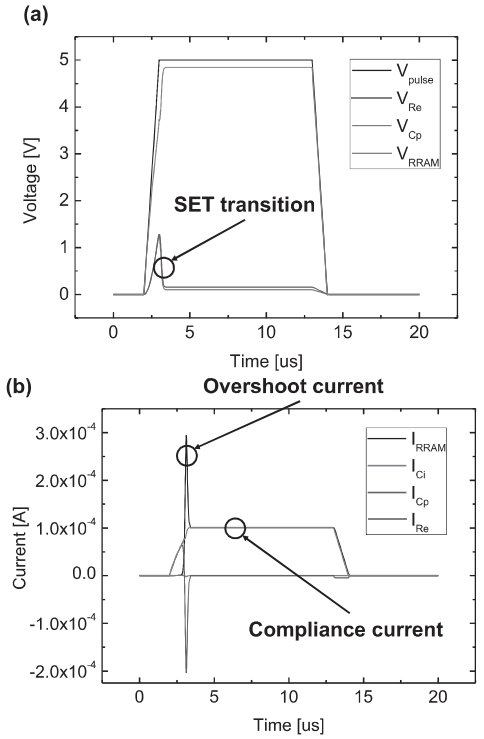

Fig. 2. Transient characteristics of single RRAM circuit. (a) Voltage changes in critical elements, (b) Current changes in critical elements

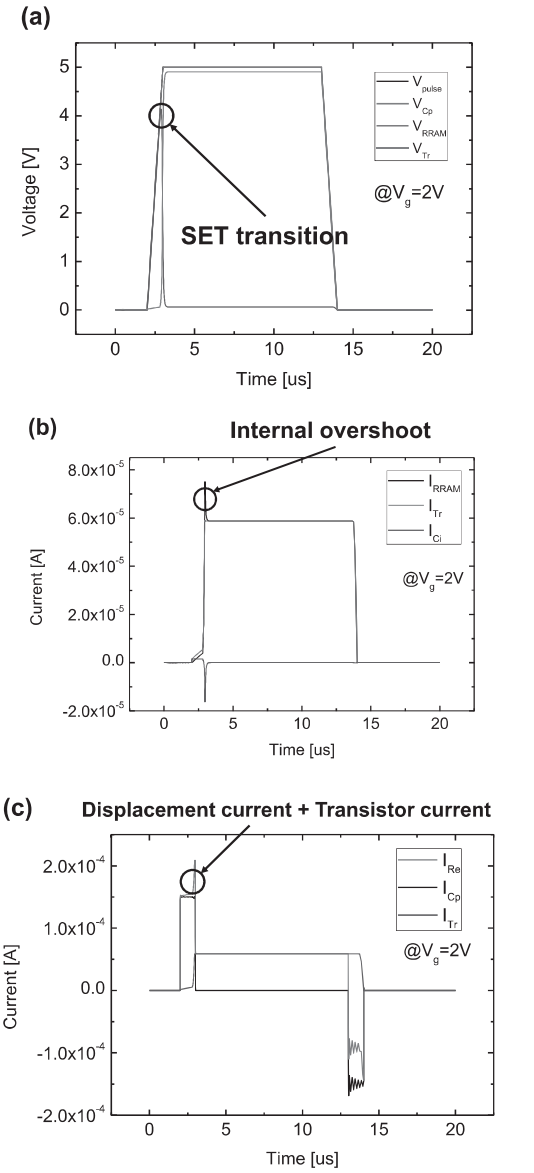

Fig. 3. Transient characteristics of 1T1R circuit. (a) Voltage changes in critical elements, (b) Current changes in internal elements, (c) Externally observed current.

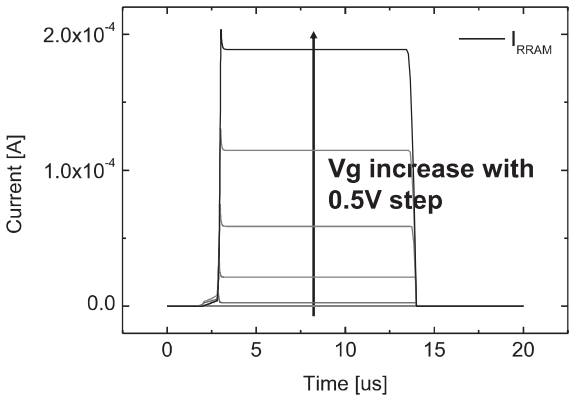

Fig. 4. Compliance current control with V_g adjusting.